I. **In the Specification**

After the title, on page 1, please delete lines 1-3 concerning related applications and insert:

— Related Applications

This application is a continuation of U.S. Patent Application Serial No. 09/010,337, filed January 21, 1998, which is related to an application titled "A Programmable Logic Block in an Integrated Circuit, Serial No. 09/010,335, file January 21, 1998, now Patent No. 6,075,381. --

On Page 6, line 3: Delete "ASCI" and insert "ASIC".

II. **In the Abstract**

Please replace the original Abstract with the following:

— "An application specific integrated circuit has at least one standard cell, integrated circuit connection circuitry connected to the at least one standard cell and at least one programmable circuit that is connected or selectively connectable to the integrated circuit connection circuitry. The selected connection is made by metal mask changes if and when it is desirable to change the logic of the application specific circuit. The programmable circuit is a general-purpose logic block and may be reprogrammed to effect design changes."—

The Abstract and, *a fortiori*, any amendments to it, shall not be used in construing the scope of the claims. MPEP § 608.01(b).

III. **In the Claims**

Please delete claims 1-19.

Please add the following new claims 20-38.

20. A method for modifying the logic of an application specific integrated circuit having integrated circuit connection circuitry connecting a plurality of standard cells and having at least one metal layer comprising:

locating at least one programmable circuit on a die before the metal one stage in two or more examples of the application specific integrated circuit, at least one of which is then provided with the at least one metal layer and at least one of which is left without the at least one metal layer;

identifying any needed design modification in the logic of the application specific integrated circuit provided with the at least one metal layer;

in the application specific integrated circuit without the at least one metal layer, connecting the at least one programmable circuit to the integrated circuit connection circuitry by providing a changed mask for and then depositing the at least one metal layer; and

configuring the at least one programmable circuit such that the needed design modification is implemented.

21. The method of claim 20 further comprising locating at least one configuration register on the die before a metal one stage, wherein the at least one programmable circuit is configured by bits stored in the configuration register.

22. The method of claim 21 wherein the configuration bits are stored in the at least one configuration register during a boot-up process.

23. The method of claim 20 wherein the act of locating the at least one programmable circuit comprises locating the at least one programmable circuit in a pattern defined by the likely location of needed design modifications.

24. The method of claim 20 wherein the act of locating the at least one programmable circuit comprises locating the at least one programmable circuit as part of a predefined, dispersed pattern.

25. The method of claim 20 wherein the act of locating the at least one programmable circuit comprises locating the at least one programmable circuit as part of a random, dispersed pattern.

26. A process for use in the manufacture of application specific integrated circuits comprising the steps of:

providing an in-process semiconductor wafer that lacks a metal one layer and on which has been formed a plurality of circuits that comprise a logic design and at least one programmable circuit;

determining whether modifications to the logic design are desired by examining a completed specimen of the application specific integrated circuits with a metal one layer;

determining desired changes in the metal one layer needed to implement the modifications in logic design, including connecting the at least one programmable circuit to the plurality of circuits; and forming a metal one layer on said in-process semiconductor wafer different from the metal one layer of the completed specimen to effect the desired changes.

27. The process of claim 26, wherein the act of connecting the at least one programmable circuit comprises interconnecting the plurality of circuits by integrated circuit connection circuitry and connecting the at least one programmable circuit to the integrated circuit connection circuitry.

28. The process of claim 26, further comprising locating at least one configuration register on the in-process semiconductor wafer.

29. The process of claim 28 further comprising storing data for configuration signals in the at least one configuration register.

30. The process of claim 26, wherein the act of providing an in-process semiconductor wafer with at least one programmable circuit comprises providing at least one general purpose logic block that comprises the at least one programmable circuit.

31. The process of claim 26, wherein the act of determining whether modifications to the logic design are desired comprises testing a semiconductor wafer upon which the plurality of circuits have been interconnected by integrated circuit connection circuitry.

32. The process of claim 26, further comprising providing on the in-process semiconductor a configuration register for storing configuration information for the at least one programmable circuit.

33. The process of claim 26, wherein the act of providing an in-process semiconductor wafer with at least one programmable circuit comprises providing a plurality of general purpose logic blocks in a dispersed pattern on the wafer.

34. A process for use in the manufacture of semiconductor device for design changes to be made by metal one level changes, said process comprising the steps of:

providing an in-process semiconductor device having a plurality of standard cells that comprise a logic design when connected by a metal layer and having at least one programmable circuit;

determining whether the logic design should be modified by testing a completed specimen of the semiconductor device with a first metal one layer;

determining changes in the first metal one layer to make a second metal one layer that connects the at least one programmable circuit as part of the logic design; and

forming a metal one layer on said in-process device to make the second metal one layer.

35. A process for use in modifying the logic of an integrated circuit, said process comprising the steps of:

providing an integrated circuit constructed on a semiconductor substrate, said integrated circuit having a plurality of standard cells that comprise a logic design and a plurality of programmable circuits dispersed on the substrate and operatively connected by a metal mask to the standard cells but programmed to have no logical effect on input signals to the programmable circuits;

determining by testing whether the logic design should be modified and identifying a modification location; and

selectively reprogramming at least one programmable circuit in proximity to the modification location to have a logical effect on its input signals that effects modification of the logic design.

36. The process of claim 35 wherein the step of providing an integrated circuit constructed on a semiconductor substrate comprises providing an integrated circuit having a plurality of programmable circuits dispersed on the substrate in a random pattern.

37. The process of claim 35 wherein the step of providing an integrated circuit constructed on a semiconductor substrate comprises providing an integrated circuit having a plurality of programmable circuits dispersed on the substrate in a predefined pattern.

38. The process of claim 35 wherein the step of providing an integrated circuit constructed on a semiconductor substrate comprises providing an integrated circuit having a plurality of programmable circuits dispersed on the substrate with a proximity focus on an area where the logic is not considered fully reliable.

IV. Payment of Fees

This Preliminary Amendment is being filed with a Request for a Continuation Application under 37 CFR §1.53(b).

A check is enclosed herewith in the amount of $690.00 for payment of the filing fee for the Continuation Application.

It is believed that no additional fees are due in connection with this communication. However, the Office is hereby authorized to charge any deficiency, or credit any overpayment to Deposit Account 04-1420.

Respectfully submitted,

Date: Sept. 28, 2005

By

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